Claims

1. A method for producing a plurality of semiconductor chips (20), particularly radiation-emitting semiconductor chips, each having at least one epitaxially produced functional semiconductor layer stack (51), comprising the following method steps:
- preparing a growth substrate wafer (1) substantially comprised of semiconductor material from a semiconductor material system that is in terms of lattice parameters the same as or similar to that on which a semiconductor layer sequence (5) for the functional semiconductor layer stack (51) is based,
- forming in said growth substrate wafer (1) a separation zone (4) disposed parallel to a main face (100) of said growth substrate wafer (1),
- joining said growth substrate wafer (1) to an auxiliary carrier wafer (2),
- detaching along said separation zone (4) a portion (11) of said growth substrate wafer (1) that faces away from said auxiliary carrier wafer (2) as viewed from said separation zone (4),
- forming on the portion (12) of said growth substrate wafer remaining on said auxiliary carrier wafer (2) a growth surface (121) for subsequent epitaxial growth of a semiconductor layer sequence (5),
- epitaxially growing said semiconductor layer sequence (5) on said growth surface (121),
- applying a chip substrate wafer (7) to said semiconductor layer sequence (5),
- detaching said auxiliary carrier wafer (2), and
- singulating the composite composed of said semiconductor layer sequence (5) and said chip substrate wafer (7) into mutually separate semiconductor chips (20).

2. The method according to claim 1, wherein prior to the application of said chip substrate wafer (7), said semiconductor layer sequence (5) is structured into a plurality of epitaxial semiconductor layer stacks (51) disposed side by side on said auxiliary carrier wafer (2).

3. The method according to claim 2, wherein at least sidewalls of said epitaxial semiconductor layer stack (51) are provided at least partially with passivating material (9).

4. The method according to at least one of claims 1 to 3, wherein prior to the application of said chip substrate wafer (7), said epitaxial semiconductor layer sequence (5) is provided with an electrical contact layer (6).

5. The method according to at least one of claims 1 to 4, wherein said separation zone (4) is produced by ion implantation.

6. The method according to claim 5, wherein hydrogen is implanted.

7. The method according to at least one of claims 1 to 6, wherein the portion (11) of said growth substrate wafer (1) facing away from said auxiliary carrier wafer (2) as viewed from said separation zone (4) is thermally cleaved along said separation zone (4).

8. The method according to at least one of claims 1 to 7, wherein said auxiliary carrier wafer (2) is transparent to electromagnetic radiation with wavelengths below 360 nm.

9. The method according to at least one of claims 1 to 8, wherein said auxiliary carrier wafer is transparent to high-energy electromagnetic radiation, particularly laser radiation.

10. The method according to claim 9, wherein said auxiliary carrier wafer (2) is detached from said semiconductor layer sequence (5) or from said semiconductor layer stack (51) by a laser liftoff process.

11. The method according to at least one of claims 1 to 10, wherein said auxiliary carrier wafer (2) is matched in terms of thermal expansion coefficient to said growth substrate wafer (1).

12. The method according to at least one of claims 1 to 11, wherein said auxiliary carrier wafer (2) is polycrystalline.

13. The method according to at least one of claims 1 to 12, wherein the joint between said growth substrate wafer (1) and said auxiliary carrier wafer (2) is produced by means of silicon oxide.

14. The method according to at least one of claims 1 to 13, wherein said semiconductor layer sequence (5) includes at least one semiconductor layer based on GaN and the material of said growth substrate wafer (1) is also based on GaN.

15. The method according to claim 14, wherein said auxiliary carrier wafer (2) is composed of sapphire and/or AlN.

16. The method according to at least one of claims 1 to 15, wherein said growth surface (121) is prepared for the epitaxial growth of said semiconductor layer sequence (5) by etching and/or grinding.